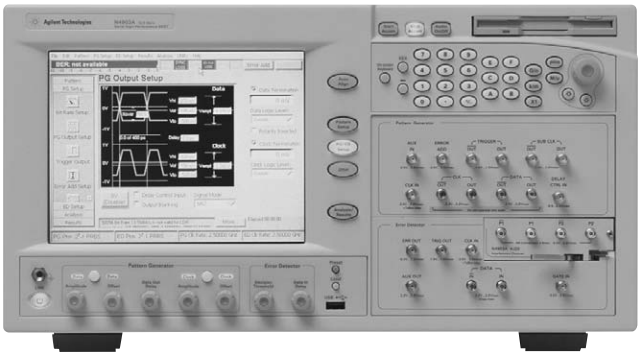
# Second Generation PCI Express® Testing with the J-BERT N4903A High-Performance Serial BERT

Application Note
Version 2.0

## Includes:



- **J-BERT sub-rate clock used for PCIe reference clock**
- **J-BERT pattern sequencer enables PCIe™ loop-back mode**
- **J-BERT measurements characterize TX performance**
- **J-BERT measurements characterize RX performance**



Agilent Technologies

**This document focuses on physical layer testing of the transmitter (TX) and receiver (RX) ports of PCI Express (PCIe™) devices. BER testing not only checks the device or chipset function, with the proper setup, it can also test transmitter and receiver parametric capabilities. This provides important information for the chipset designer.**

**This document highlights how to implement a total BER test solution with the Agilent J-BERT N4903A High-Performance Serial BERT. It provides details on how to set the equipment up, for example, for pattern editing, and explains the capabilities for functional and parametric test including jitter injection for jitter tolerance tests.**

## PCI Express Background

The PCI Express (PCIe) bus is no longer a parallel data bus through which all data is routed at a set rate. Rather, an assembly of serial, point-to-point, individually clocked 'lanes', each consisting of two pairs of differential data lines, one carrying data upstream and one downstream. The lanes can be stacked together to increase the bandwidth available to specific areas of the I/O system, such as the video card slot, for example (see Figure 1).

For the 2nd generation of the technology, each lane is capable of a 5 Gb/s data rate in each direction.

This technology has a couple of immediate benefits. For example, point-to-point circuitry reduces the number of trace routes on a motherboard considerably. The biggest impact that PCIe has made on the desktop PC market is with the PCIe x16 graphics slot. This implementation of the technology has replaced AGP 8x as the platform of choice for graphics card manufacturers.

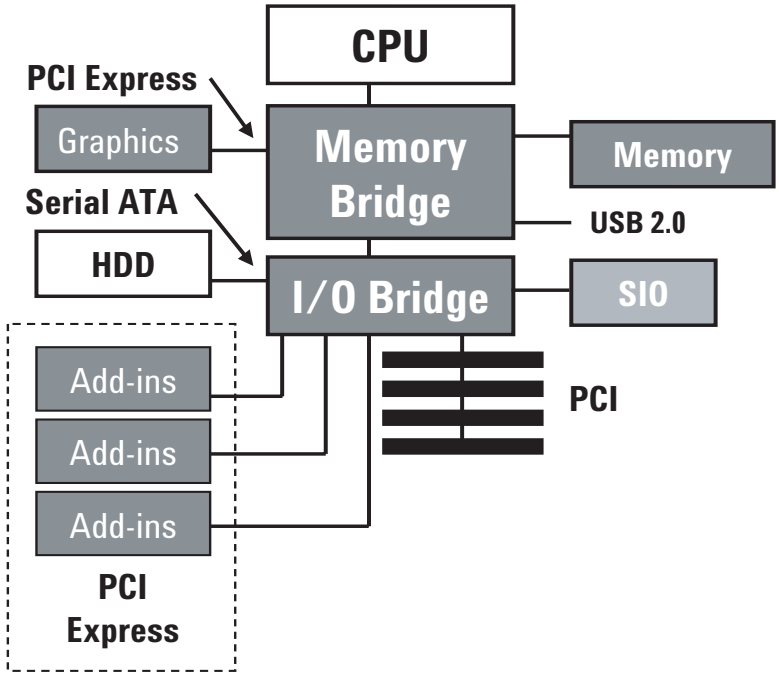



**Figure 1: Motherboard structure**

## PCIe physical layer specifications

PCIe increases data transport efficiency and data quality. It uses 8b/10b-encoding to embed the clock signal into the data signal. There can be up to 16 lanes. In the 1st generation, the data rate is 2.5 Gb/s [1]. The 2nd generation doubles the speed and adds further signal integrity requirements [2], which places new demands on jitter testing. Again, it is designed for a Spread Spectrum Clock (SSC) to reduce electromagnetic interference (EMI) issues.

A brief look at the specifications clarifies the test margins. The PCIe chipset includes a transmitter (TX) and a receiver (RX). Each has different physical parameters defined by the standard [1, 2]. Figures 2, 3 and 4 provided here are copies from the standards for the 2nd generation [2].

## Characterizing the TX

For the TX, the data stream is at 5 Gb/s, which means a unit interval (UI) of 200 ps. The data rate may vary by ±300 ppm, not including the SSC, which adds a triangular modulation of -0.5% at a rate of 30 kHz.

The PCIe 2nd generation specification defines two voltage swing levels: full swing and low swing. Full swing signaling uses de-emphasis, while low swing does not. Whether a transmitter needs to support full swing, low swing, or both modes depends on how it is being used. Typically, low swing is used for power sensitive applications where a shorter channel is acceptable.

The method by which the output mode is selected is not explicitly defined in the specification, and may be made dependent on the implementation.

## Characterizing the RX

The other part of the PCIe physical system is the RX. Again, the data rate is 5 Gb/s, or a UI of 200 ps, with ± 300 ppm timing variation. While two different TX signaling levels are defined, there is only a single RX voltage level specification. This means the margins specified at the RX are independent of the TX's output swing. It also means the channel characteristics need to be matched to the TX output swing. Typically, low swing output will support a channel with roughly half the loss supported by full swing signaling.

The Compliance Eye Test requires the input signal to be down to 120 mV in differential amplitude and closed to 0.4 UI in time (see Figure 2). For the Receiver Dynamic Voltage Range the input voltage required should provide a dynamic range of Vswing_max / Vswing_min = 5 and a minimum Pulse Width down to .6 UI (see figure 3).

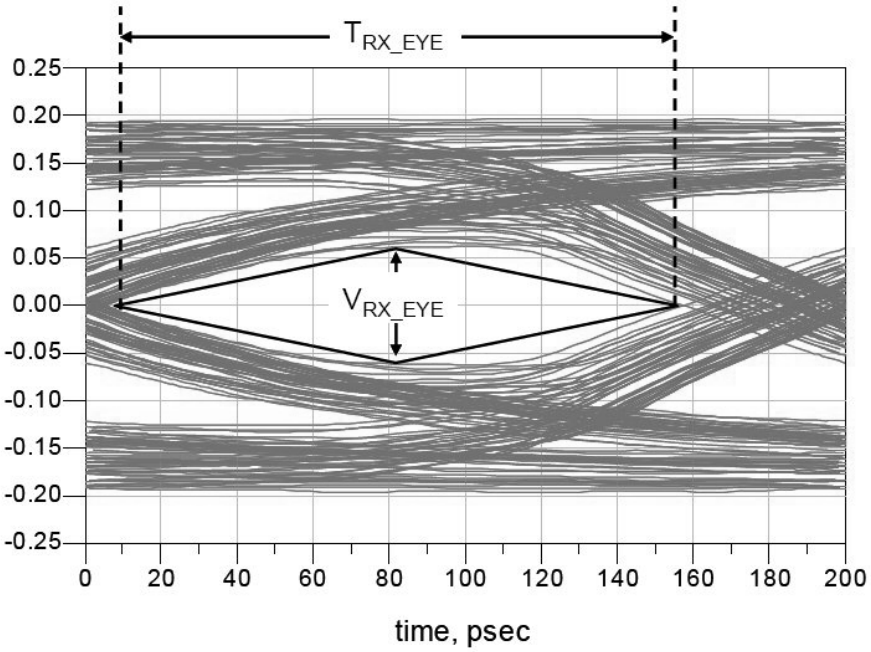



**Figure 2: Receiver eye margin, on the differential signal, according to PCIe base standard [2]**

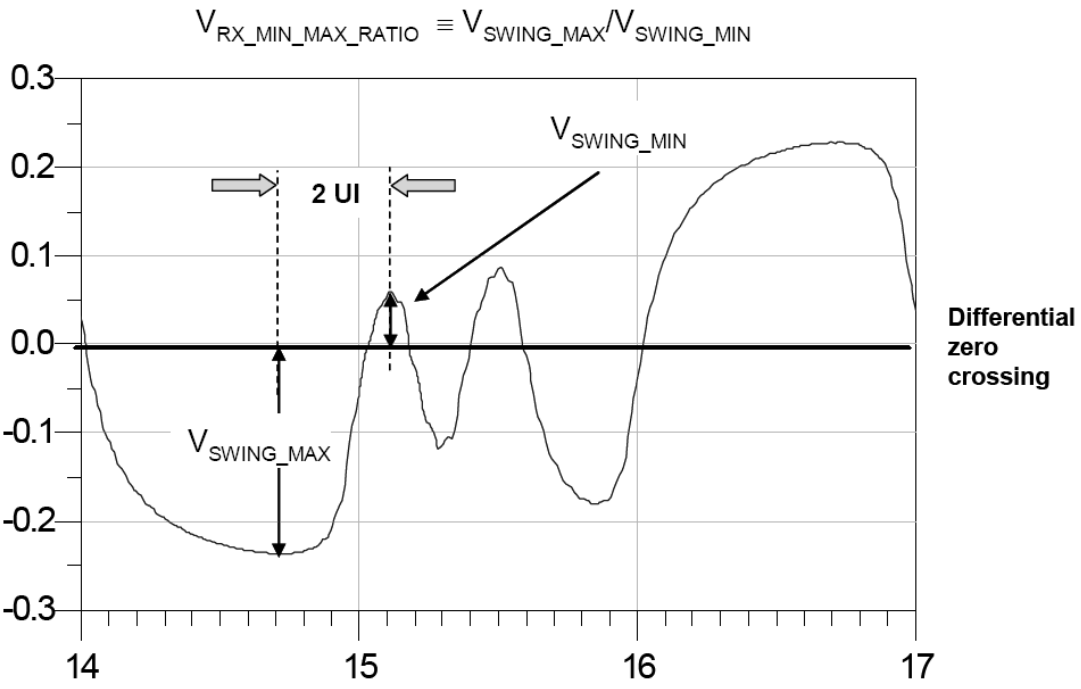



**Figure 3: Receiver Dynamic Voltage Range**

The difference between RX and TX amplitude and timing specification is the budget for jitter allowed in the media between two chipsets.

The RX must be able to resolve inputs with substantially differing amplitudes that arise from channel Inter-Symbol Interference (ISI). This is expressed with a VRX-MAX-MIN-RATIO with a value of 5 (see Figure 3). This corresponds to a transmission line length of 25 inches over conventional FR4 material.

In addition, the RX input must tolerate an AC peak common mode input voltage of up to 150 mV.

The 2nd generation receiver is characterized by meeting a Bit Error Ratio (BER) for a specified set of worst-case input conditions, as defined in the specification [2]. The receiver specification is compatible with an easily implemented test setup. It is not possible to measure at the pins of a receiver directly, because such a measurement would consist of both incident and reflected signal components. This problem is overcome by adjusting the receiver parameters to meet worst-case specification margins when measured into a reference load, and then substituting the receiver under test in place of the load. A two-step approach allows accurate adjustment of receiver test conditions and decouples the receiver's electrical parasitics from the setting of the worst-case corner conditions.

In developing the RX specification margins, allowance was for signal degradation between what is measured at the reference load and what is needed at the receiver device pads. The designers of the RX silicon and packaging need to design for package-silicon interactions that guarantee signal levels at the device's pads will yield a good enough BER.

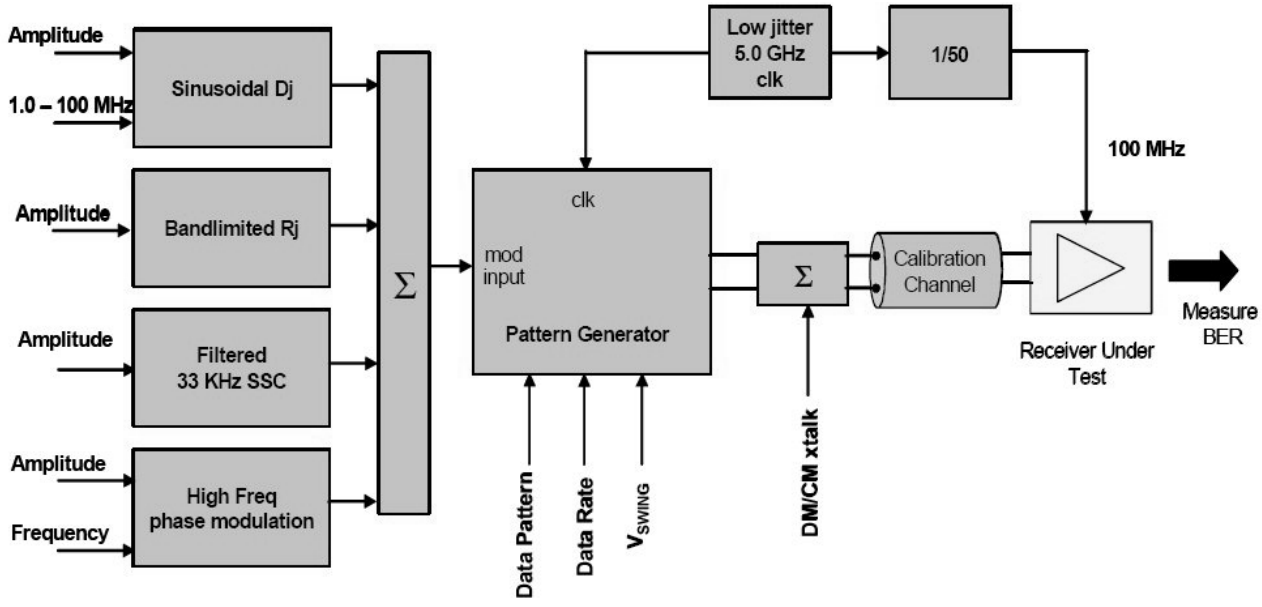



**Figure 4: Setup for testing the receiver, according to [2] (not an actual implementation)**

## PCIe test basics

PCIe includes three layers altogether: at the bottom there is the "physical layer", above this is the "data link layer" and on top is the "transaction layer". Each layer needs proper instrumentation for validation and verification. For the physical layer, a pattern generator and error detector, and an oscilloscope are usually used to check proper bit error ratio (BER) and signal integrity. A logic analyzer helps validate the data link layer, as well as being useful for code debugging. A protocol analyzer and exerciser can be used to validate the transaction layer.

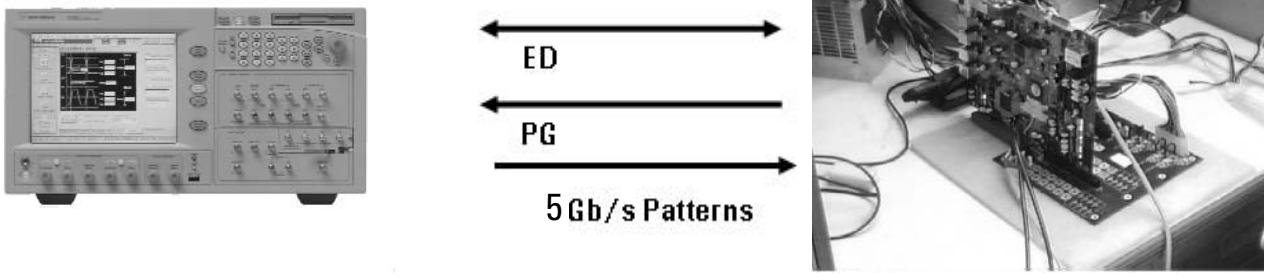
## PCIe physical layer environment and test setup

PCIe physical layer testing can be performed in two ways. First there is motherboard testing and second there is the add-in card test (see Figure 5). Motherboard testing focuses on North Bridge or South Bridge chipsets placed on a motherboard. This needs a solution like the compliance load board (CLB) to access the signals for TX and RX. Testing of add-in cards, like Ethernet or graphic cards, should use the compliance base board (CBB) to access the TX and RX signals [3]. The CBB needs to be powered from a regular PC power supply, and the motherboard normally provides the 100 MHz reference clock. For add-in card testing this needs to be provided from the test setup.

## PCIe BER test principle

Testing the bit error ratio (BER) of a digital data stream uses the following basic procedure. First, a pattern generator sends a bit stream to the DUT (device under test). The error detector internally produces a bit stream called expected data, based on the bit stream sent by the pattern generator, but depending on the DUT, possibly different from it. The bit stream from the DUT output is fed back to the error detector. After digitizing and sampling, the decision circuit in the error detector compares the incoming bit stream against the expected data, bit-by-bit, in real-time. If corresponding bits are different, this is counted as an error. The bit error ratio is the number of errors for the total number of bits compared. This is the basic principle of BER testing, which can be applied to different applications, such as optical transceiver test, digital IC chip test, or digital communication system test. BER testing needs a known, deterministic and periodic bit stream that runs through the DUT. To make BER testing possible for PCIe devices, the standard defines a loop-back mode. To put the DUT into loop-back mode, specific symbols need to be sent within Training Sequences TS1 and TS2.

**Figure 5: PCIe graphics card on the compliance base board**



The training sequences are part of the configuration when a PCIe Link starts running from a valid hot plug-in (see Figure 6). In this setup the PCIe device runs through "Detect State" into "Polling State", then "Configuration State" and finally into "L0" mode by exchanging TS1 and TS2, including specific link information. To force the DUT into loop-back mode it is necessary to send a stream of TS1 and TS2 with the loop-back bits of symbol 5 enabled. Once in loop-back mode, most bit sequences can be used, as long as they use valid 8b/10b coding. This allows any functional and parametric verification or compliance testing based on the BER measurement.

## Creating the proper training sequence flow

As described earlier, BER testing is a matter of individual bits. Training Ordered Sets needed here are based on symbols, which is a bit stream based on the rules of:

- The Running Disparity of the 8b/10b Coding
- The Skip Ordered Set
- Proper repeating of the trai ning ordered sets

On the BER test equipment, this will be setup by using the sequence and segment editing.

## Test Equipment

The focus of this document is on a test solution for the physical layer test of PCIe using the Agilent Technologies J-BERT N4903A High-Performance Serial BERT (shown in Figure 6) with complete jitter tolerance testing capabilities. The jitter injection capabilities are outlined in Figure 8.

Important is the capacity of this BER tester (BERT) to modulate the clock for the timing. This enables UI jitter at frequencies below 4 MHz, or the creation of a Spread Spectrum Clock (SSC). For higher jitter frequencies (up to 1 GHz) there is a voltage controlled Delay Line where any external signal can be applied.

For PCIe, this can be modulated by a mixture of a sinusoidal signal (Pj), Random Noise (Rj), and bounded Random Noise (BUJ). Finally the data signal can be conditioned with Inter-Symbol Interference (ISI) and noise can be added in common or differential mode.

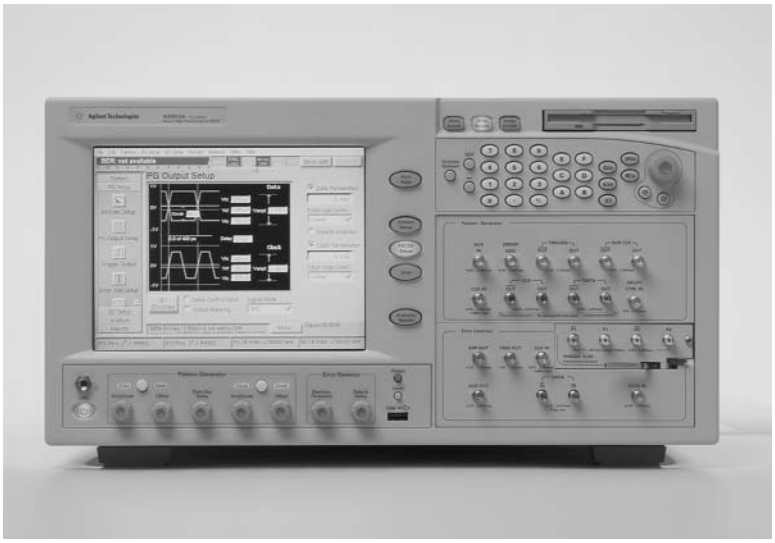



**Figure 6: Agilent J-BERT N4903A High-Performance Serial BERT with jitter tolerance testing capabilities**

## Recommended configuration

The base system is available as J-BERT #C07 or #C13.
#C07 runs up to 7 Gb/s, #C13 up to 12.5 Gb/s.
#J10 adds the jitter sources SJ, PJ, RJ & BUJ
#J11 adds the capability for SSC
#J20 adds the Interference channel with ISI and SI which adds common and differential noise to the data output.

Another recommended option is #A01, which adds the Bit Recovery Mode. Bit recovery is a method of testing BER without setting up expected data. The data from the DUT is taken as reference. This capability is described in detail in [4].

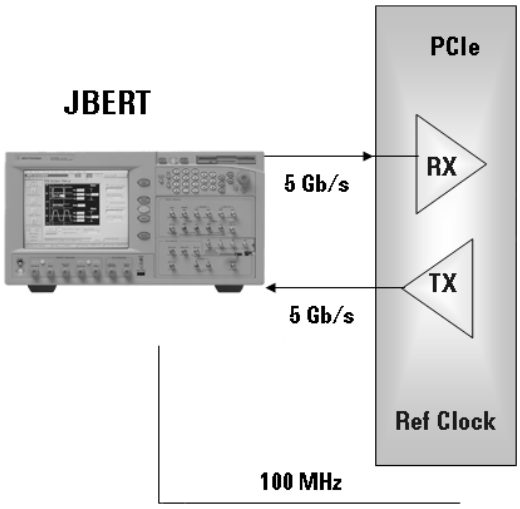



**Figure 7: Setup of J-BERT with PCIe DUT**

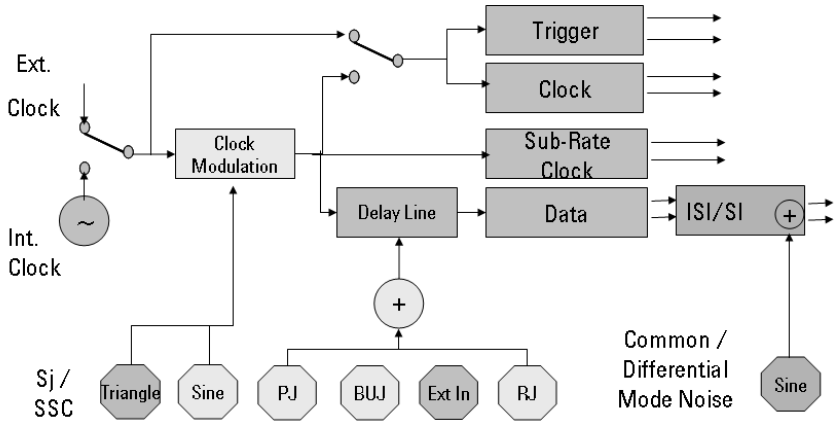



**Figure 8: Architecture of jitter capabilities of the Agilent J-BERT N4903A High-Performance Serial BERT**

## J-BERT setup

**1.Frequency**
The generator and analyzer are set to a data rate of 5 GHz.

**2.Reference Clock**
Ref Clk is connected to the divided clock output; the divider is set for 50 to generate a 100 MHz clock.

**3. Signal into RX:**
Data out is connected differentially to RX. For a functional test, 1 Vdiffpp is used. As the differential amplitude is twice the single ended amplitude, the DC levels are HIL = +0.25 V and LOL = -0.25 V, and the termination voltage, Vt, is 0 V.

**4**.There is a choice of using either the external clock from the data generator or the built-in clock-data recovery (CDR) for the analysis. Using CDR has the advantage that, when testing for jitter, low frequency effects are tracked by the CDR and omitted from the jitter numbers. For SSC testing it is recommended to run the analyzer on the external clock provided by the generator, to keep the test system in phase with the SSC clock.

**5.**Figure 9 shows the Sequence Editor with the pattern setup for loop-back mode. This combines loops and customized user patterns. It shows the setup of the necessary TS1 and TS2 flow with embedded SKIP symbol generation. SKIP symbols are required regularly. Here they are provided by the TS1SKP and TS2SKP segments. This forces the PCIe device into loop-back mode. Once in loop-back mode, the COMPLIANCE pattern, with length of 40 bits, is looped infinitely for BER testing.

The compliance pattern is also assigned to the error detector as expected data.The sequence editor is set to "Start on Command". This can be selected from the Sequence Editor Properties.
The advantage of this is the BERT's internal clock generation is already active and the generators subrate clock is running before hitting the START button. The PCIe DUT needs the reference clock running for a while to get its internal PLL up and running before the training sequences are applied.

## Test results

The following test results were obtained from a 1st generation PCIe graphic card connected with the CBB (compliance base board).

## RX/TX functional test:

For the functional test, the sequencer is started and the error detector performs an 'Auto Align'. The result is shown in Figure 10. The eye-opening is reported and the BER reading is zero.

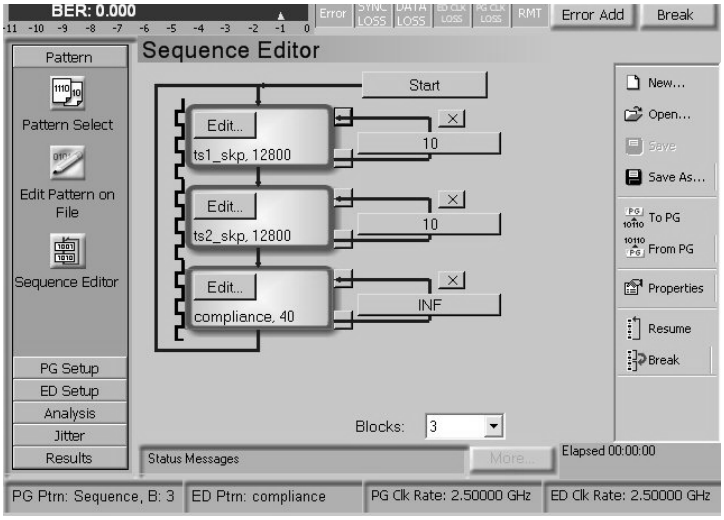



**Figure 9: Sequence editor for training and BER test**

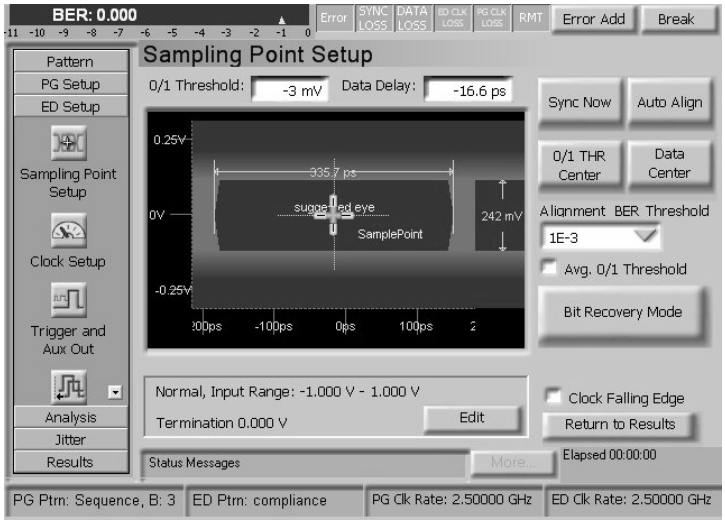



**Figure 10: Sampling point setup**

## TX output measurements

### TX output jitter

The TX timing performance is obtained with help of the output timing measurement, as shown in Figure 11. This provides jitter measurement including RJ/DJ separation. Besides the phase margin reading, which is taken at the actual BER threshold, there is an extrapolation for total jitter (Tj) for a BER threshold at 1e-12. This extrapolated value is 112 ps.

A real measurement down to 1e-12 is provided by the Fast Total Jitter Measurement, shown in Figure 12. This tool measures the real BER. In this case, the measured value is 114 ps - very close to the extrapolated value. Therefore, the much longer measurement time for the full measurement should be needed only once; there is no need to perform this again for parameter variations.

## TX output level

Measuring output level, as shown in Figure 13 provides level and amplitude information for the differential output signal. The measurement provides a direct reading of the differential levels and amplitude as a function of BER. There are also readings for level and amplitude noise and finally, because this measurement can also be used for optical outputs too, a calculation for the Q factor is also provided.

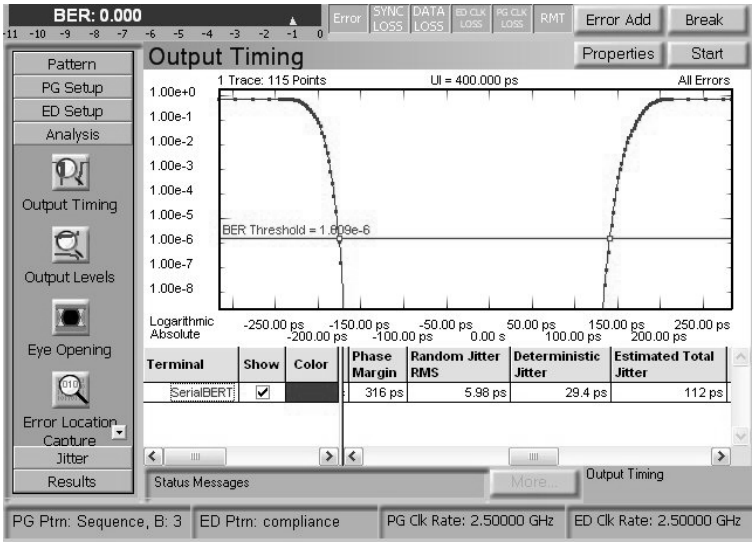



**Figure 11: Output timing measurement**

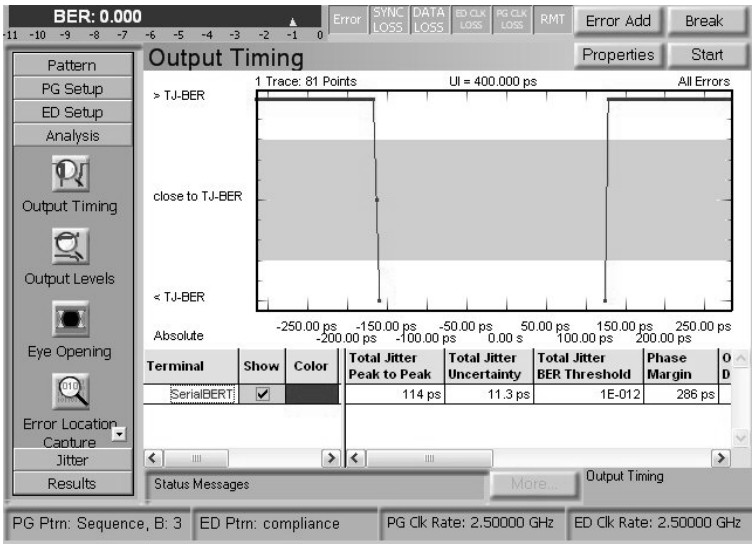



**Figure 12: Fast Total Jitter measurement**

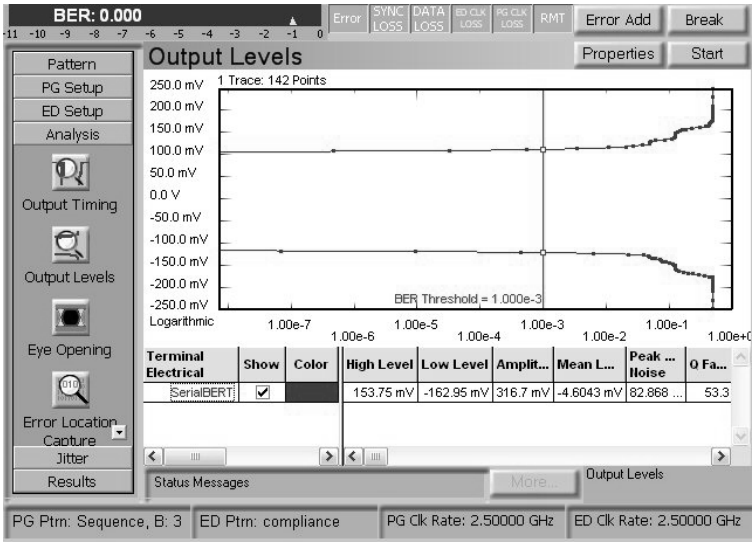



**Figure 13: Output level measurement**

## TX output eye

The eye-opening measurement provides the eye contour in time and voltage for the differential signal, as shown in Figure 14.

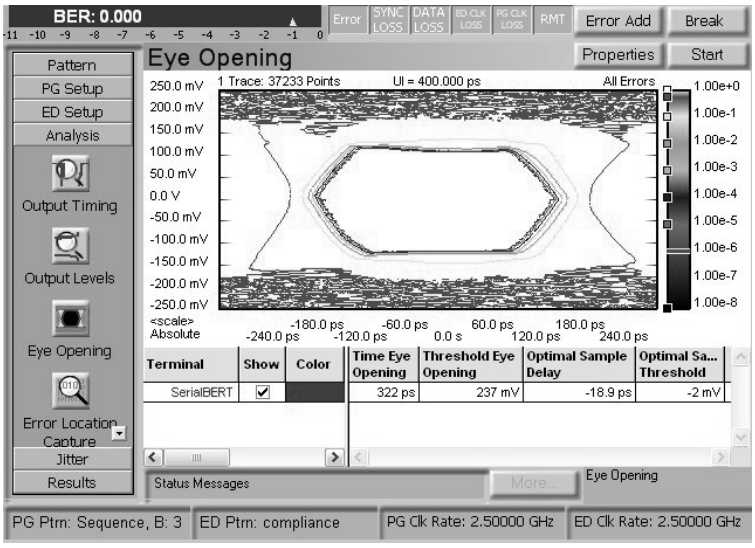



**Figure 14: Eye diagram as two dimensional BERT Scan**

## TX jitter spectrum

The spectral decomposition, as shown in Figure 15, is a useful debug tool. This provides insight to the spectral content of jitter and can be helpful in identifying the sources and root-causes of jitter. From the measurement we can make the following observations:

- There is a peak at around 2 MHz. This is phase noise, most likely generated in the clock generation and distribu tion.
- The compliance pattern repe ats every 40 bits, so the lowest pattern frequency is 67.5 MHz. All the needles between 67.5 MHz and maximum speed are due to data dependent jitter.
- There are two more peaks between 5 and 10 MHz. These are most likely caused by crosstalk.

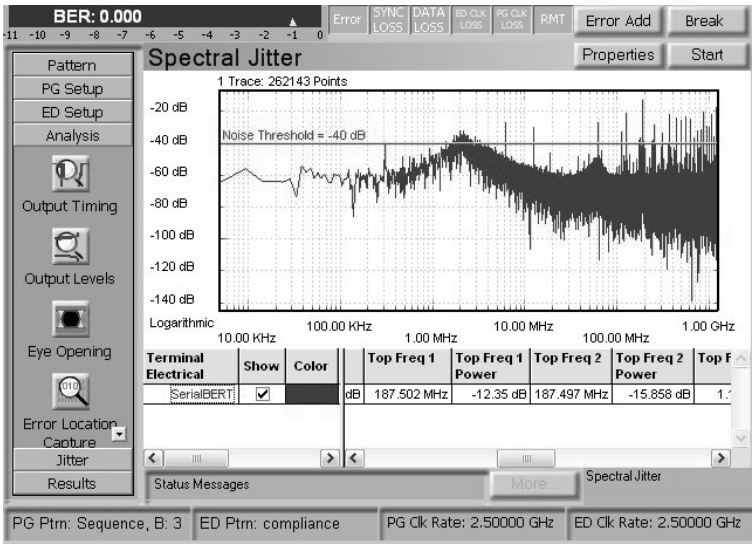



**Figure 15: Spectral jitter decomposition**

## Receiver RX input measurements

To check the parametric behavior of the RX input, we need to create:

- the Receiver Compliance Eye - worst case
- the waveform for Receiver Dynamic Voltage Range

In the words of the standardization body, the J-BERT is the 'Receiver Test Circuit' and the 86100C Infiniium DCA-J is the 'Test Load' with built-in display. The J-BERT including the jitter options has built-in all jitter sources (as indicated in figure 8) required by the specification (as shown in figure 4).

Noise is added to create the Receiver Compliance Eye common mode. The data signal needs to be modulated with Bounded Uncorrelated Jitter (BUJ) and Sinusoidal Jitter (Sj/Pj) to create an eye closure down to .6 UI, which corresponds to a minimum eye opening of .4 UI.

To add common mode noise the data signal is fed through the ISI/SI plug-in with the shortest ISI path enabled. This provides filtering of the steep edges to more sinusoidal behavior. Common mode noise of 150 mV at 2.5 GHz and bounded uncorrelated jitter (BUJ) of .16 UI is added. Then with periodic jitter (PJ) the eye is closed to .6 UI. Finally the generator's amplitude is adjusted for a vertical opening of 120 mV of the differential amplitude, as shown in figure 16. The amplitude of the single ended signal is 60 mV. The setup of jitter mix is shown in figure 17.

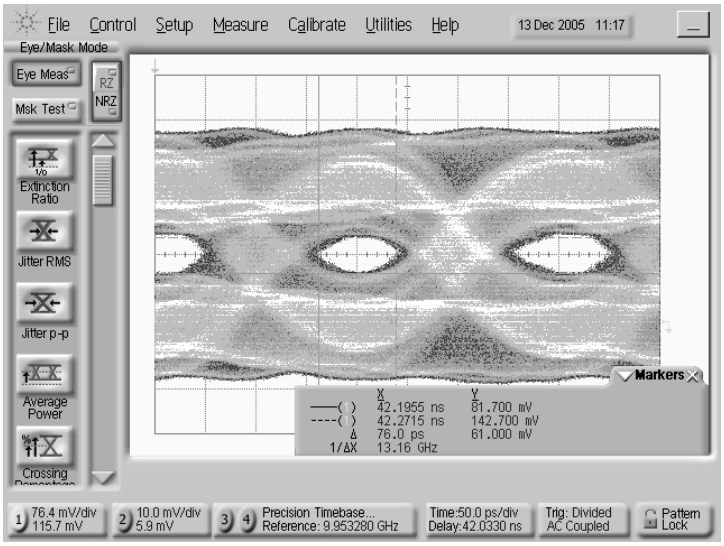



**Figure 16: Scope Shot (single ended) BUJ/PJ modulated waveform with Common Mode noise of 150 mV**

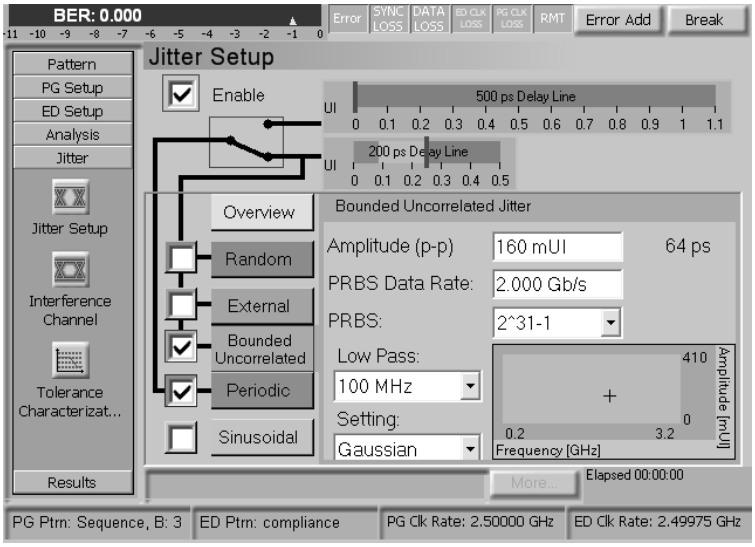



**Figure 17: Jitter Setup of J-BERT for Compliance Eye**

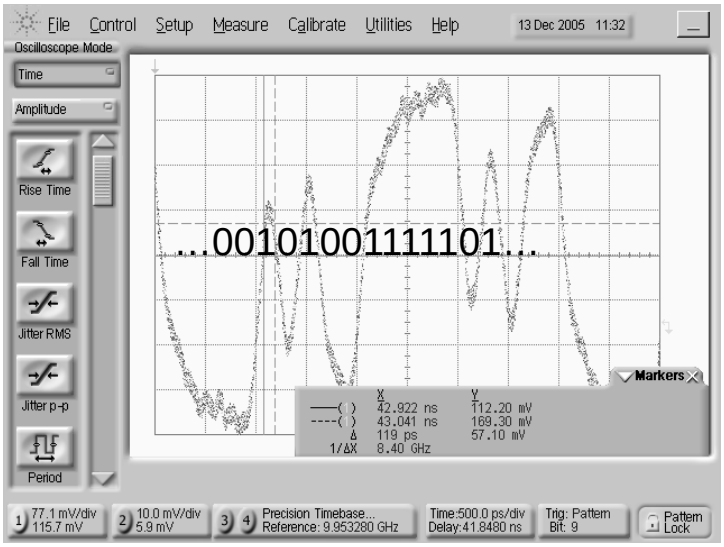



**Figure 18: Scope Shot (single ended) ISI modulated waveform with Differential Mode noise**

To create the waveform for the Receiver Dynamic Voltage Range the ISI filter is used together with the addition of differential mode noise. Pattern wise, this is performed ideally with the bits of the Comma Symbol; a single one/zero is following 5 consecutive identical bits.

The appropriate ISI filter shall provide an amplitude ratio of 1/5 for Vswing_min / Vswing_max. This is achieved best with trace 3 of the programmable filter. Then differential mode noise is added adjusting the minimum pulse width of the single bit for a pulse width of .6 UI. Finally the pattern generator's amplitude is adjusted for a vertical opening of 120mV for the single bit. The resulting signal is shown single ended in figure 18.

Figure 19 shows the setup of the ISI filter and the addition of differential noise.

For the characterization of the RX, it is sufficient to look for the BER figure to the signal obtained at the loop-back point. For Conformance Testing it may be desirable to load the RX input with a signal conditioned according the compliance requirements and check the TX output to the compliance requirements.

The version 0.7 of the standard for PCIe 2.0 [2] does not say much about jitter tolerance requirements, but it is expected that the next, faster implementation will require operation according to a jitter tolerance curve. This needs to be tested by sweeping the jitter frequency and magnitude from multiple UIs at low frequency to fractions of a UI at higher frequency.

At least for characterization this is a test required. The J-BERT provides an automated software tool to sweep SJ from low frequencies with multiple UIs up to high frequency PJ to record the jitter tolerance behavior. Figure 20 shows the screen shot taken from a Gen1 device. All above measurements can be performed with a J-BERT equipped with #J10 and #J20.

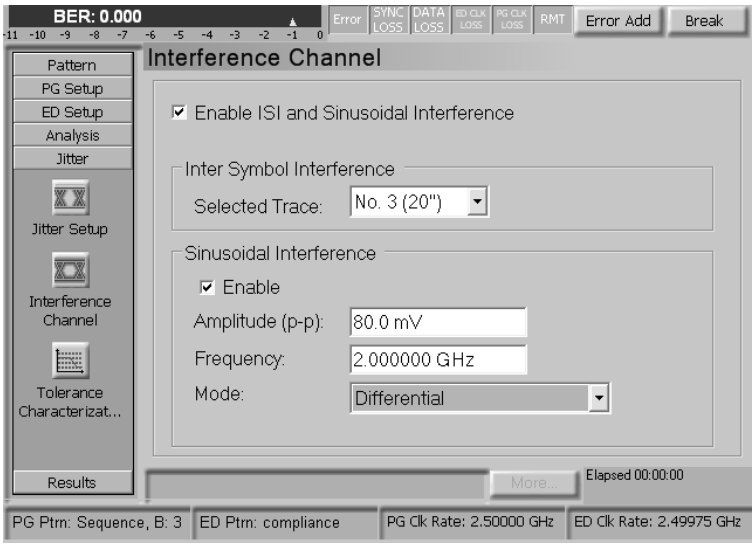



**Figure 19: Setup of J-BERT for Receiver Dynamic Voltage Range waveform**

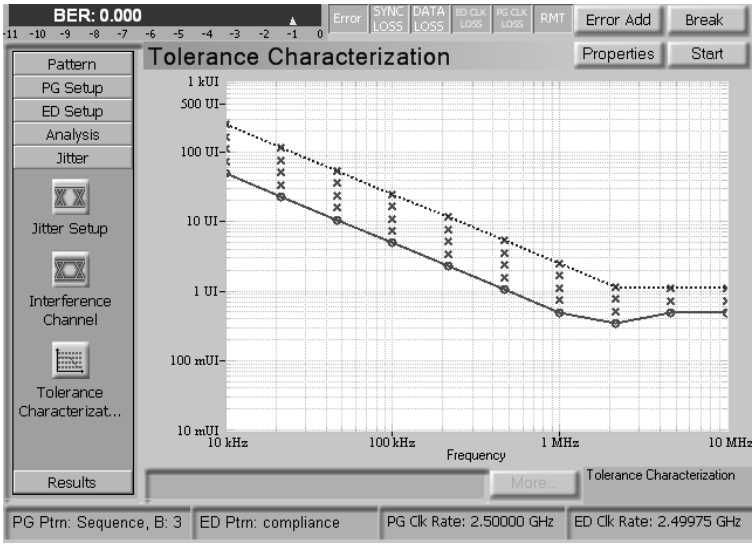



**Figure 20: Jitter Tolerance Characterization**

## Spread Spectrum Clocking

The PCIe standard states that the data rate can be modulated from +0% to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30 kHz - 33 kHz, while the modulating signal is triangle shaped. The ± 300 ppm frequency requirement has to be maintained, which requires the two communicating ports to be modulated such that they never exceed a total of 600 ppm difference. For most implementations, this places the requirement that both ports require the same bit rate clock source when the data is modulated with an SSC.

FM modulation is symmetrical. The recommended setting on the signal generator is therefore 4.9875 GHz with a modulation deviation of ±.25%, which is 12.5 MHz. On the J-BERT generator the offset shift is automatically performed when enabling the SSC. The programming is still 5 Gb/s as frequency on the Generator. Figure 21 shows the enabling on the generator timing page. For SSC generation the J-BERT requires to be equipped with #J10 and #J11. The SSC modulation is also present on the clock and sub-rate clock outputs.

The Error Detector in ext. clock mode will automatically detect the proper frequency as the median frequency. When using the CDR mode, the reference frequency has to be set to the median frequency of 4.9875 Gb/s by the user.

Figure 22 compares the Eye Opening of a PCIe 1.0 device with and without SSC. It can be seen that SSC affects the eye opening of the device. The copied waveform (always the traces to the right) represents the measurement with SSC enabled.

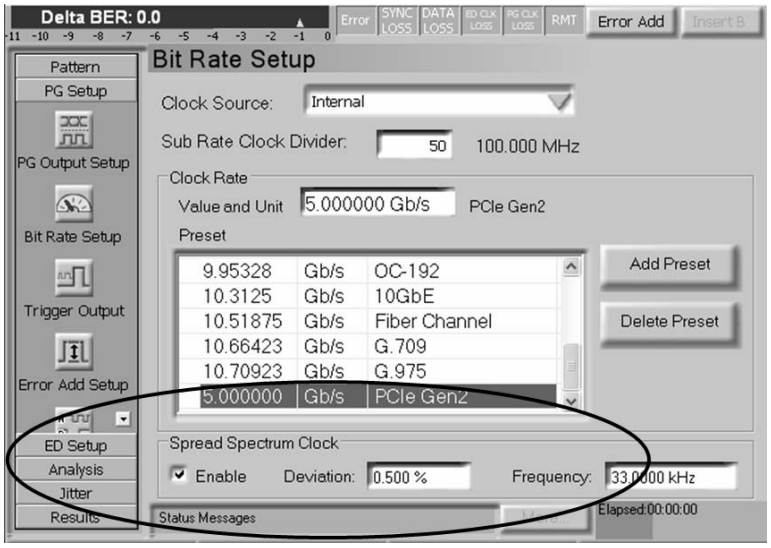



**Figure 21: Enabling the SSC Clock on the J-BERT generator**

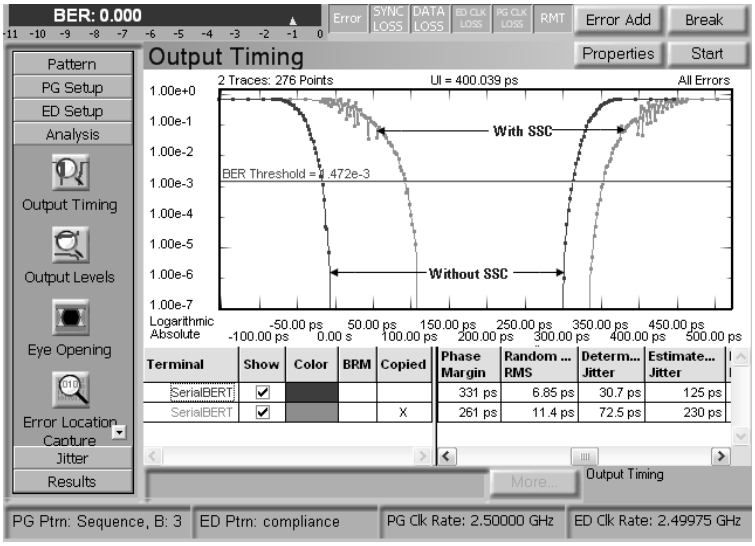



**Figure 22: Output Timing Measurement with and w/o SSC**

## Conclusions

A PCIe physical layer test solution is important for chipset designers. BER testing is becoming more and more important as the data rate increases. This is especially true for the second-generation of PCIe, as well as for SATA II/III and high-speed Fully Buffer DIMM (AMB chip) test in the future. With the J-BERT N4903A High-Performance Serial BERT Agilent offers a powerful solution for the physical layer measurement needs.

**References:**

[1] PCI Expres® Base
Specification Revision 1.1

[2] PCI Express 2.0®
Base Specification Revision 0.7,
October 2005

[3] Compliance Base Board
(CCB), Compliance Load Board
(CLB), see the link:

http://www.pcisig.com/specifi-
cations/pciexpress/complian-
ce/compliance_library

[4] Eye Characterization on Idle
and Framed Data Traffic:
the Bit Recovery Mode
Application Note 5989-3796EN

## Related Literature

J-BERT N4903A High-Performance Serial BERT Data Sheet **5989-2899EN**

J-BERT N4903A High-Performance Serial BERT Brochure **5989-3882EN**

Bit Recovery Mode Application Note **5989-3796EN**

Serial BERT Literature
**www.agilent.com/find/N4903**

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